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EXAMINER	
PERVAN, MICHAEL	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
12/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/720,847	KIMURA, HAJIME	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7,18,28,59,64,66,71-74 and 76-93* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,18,28,59,64,66,71-74 and 76-93* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/28/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 28, 2009 have been fully considered but they are not persuasive.

Applicant (on pages 10-11 of argument) argues that because a constant current is applied to the transistor there would be no motivation for changing the size of the gate width. Examiner respectively disagrees.

Even though a constant current is being applied, the size of the gate width of the transistor determines if all or only a part of the current is able to flow through the transistor similar to how the diameter of a pipe changes how much water flows in the pipe. As a result, the increasing gate width size would allow more of the constant current to flow which allows the desired precharge voltage to be reached more efficiently. Thus, the combination still reads on the claims and the rejection stands.

Applicant (on page 10 of argument) argues that the Examiner was only comparing the amount of current flow and not the size of the gate widths. Examiner respectively disagrees.

Shin shows that two transistors can have different gate widths and that the difference in the sizes between the two transistors correlates to the amount of current flow. Shin was not merely cited to show the changing the size of one transistor changes the amount of current but that the differences in size between two transistors has an

affect on the current flow as well. Therefore, the combination still reads on the claims and the rejection stands.

In response to applicant's argument that Shin does not provide the same advantages as provided in applicant's specification, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7, 18, 28, 59, 64, 66 and 71-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp et al (US 6,373,454) in view of Suzuki (US 6,369,786) in further view of Shin (US 2003/0231152).

In regards to claims 1, 71, 72, 76, 78 and 80, Knapp discloses a semiconductor device comprising:

a driven circuit (pixel block 10) comprising a first transistor (Fig. 2; transistor 30);

a signal line (I_{in}) electrically connected to the first transistor through a node (Fig. 2; as can be seen from the drawing, the first transistor (30) is connected through a node (36) to a signal line),

wherein a gate electrode of the first transistor is connected to a drain electrode of the first transistor through a first switch (32) (Fig. 2 and col. 6, lines 32-34).

Knapp does not disclose a precharge circuit electrically connected to the signal line and comprising a second transistor, and a current source circuit electrically connected to the first transistor and the second transistor, wherein a gate electrode of a second transistor is electrically connected to a drain electrode of the second transistor, wherein a gate width of the second transistor is larger than a gate width of the first transistor and wherein the precharge circuit is configured to perform a precharge of the driven circuit prior to supplying the signal current to the driven circuit.

Suzuki discloses a precharge circuit (3A) electrically connected to the signal line and comprising a second transistor (diodes D_1-D_x) (col. 5, lines 50-54), and a current source circuit (CS_{1-x}) electrically connected to the first transistor and the second transistor (col. 5, lines 50-54), wherein a gate electrode of a second transistor is electrically connected to a drain electrode of the second transistor (col. 5, lines 50-54; since connecting a transistor in such a manner causes the transistor to act as a diode, having a diode instead of a diode connected transistor would still act in the same manner), and wherein the precharge circuit is configured to perform a precharge of the driven circuit prior to supplying the signal current to the driven circuit (col. 5, line 65-col. 6, line 7).

It would have been obvious at the time of invention to modify Knapp with the teachings of Suzuki, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

Knapp and Suzuki do not disclose wherein a gate width of the second transistor is larger than a gate width of the first transistor.

Shin discloses wherein a gate width of the second transistor is larger than a gate width of the first transistor (paragraph 16).

It would have been obvious at the time of invention to modify Knapp and Suzuki with the teachings of Shin, gate width of the second transistor being larger than the gate width of the first transistor, because it allows for a greater current to flow from the precharge circuit, which allows for a faster precharge.

In regards to claims 7 and 77, Knapp does not disclose the semiconductor device according to claim 1, further comprising

an impedance transformation amplifier.

Suzuki discloses an impedance transformation amplifier (col. 5, lines 62-63).

It would have been obvious at the time of invention to modify Knapp with the teachings of Suzuki, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claims 18 and 82, Knapp discloses a semiconductor device comprising:

a driven circuit (pixel block 10) comprising a first transistor (Fig. 2; first transistor (30));

a first switch for controlling an electrical connection between the driven circuit and the precharge circuit (Fig. 2; first switch (37)); and

wherein a gate electrode of the first transistor is connected to a drain electrode of the first transistor through a switch (Fig. 2 and col. 6, lines 32-34).

Knapp does not disclose a precharge circuit comprising a second transistor, a second switch for controlling a connection between the driven circuit and a current source circuit, wherein a gate electrode of a second transistor is electrically connected to a drain electrode of the second transistor, wherein a gate width of the second transistor is larger than a gate width of the first transistor and wherein the first precharge circuit is configured to perform a precharge of the driven circuit prior to supplying the signal current to the driven circuit.

Suzuki discloses a first precharge circuit (Fig. 7; 3A) electrically connected to the signal line and comprising a second transistor (diodes D_1-D_x) (col. 5, lines 50-54), a second switch (S_1-S_x) for controlling a connection between the driven circuit and a current source circuit (Fig. 7), wherein a gate electrode of a second transistor is electrically connected to a drain electrode of the second transistor (col. 5, lines 50-54; since connecting a transistor in such a manner causes the transistor to act as a diode, having a diode instead of a diode connected transistor would still act in the same

manner), and wherein the first precharge circuit is configured to perform a precharge of the driven circuit prior to supplying the signal current to the driven circuit (col. 5, line 65-col. 6, line 7).

It would have been obvious at the time of invention to modify Knapp with the teachings of Suzuki, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

Knapp and Suzuki do not disclose wherein a gate width of the second transistor is larger than a gate width of the first transistor.

Shin discloses wherein a gate width of the second transistor is larger than a gate width of the first transistor (paragraph 16).

It would have been obvious at the time of invention to modify Knapp and Suzuki with the teachings of Shin, gate width of the second transistor being larger than the gate width of the first transistor, because it allows for a greater current to flow from the precharge circuit, which allows for a faster precharge.

In regards to claim 83, Knapp does not disclose the semiconductor device according to claim 82, further comprising a current source circuit configured to input a signal current to the driven circuit.

Suzuki discloses a current source circuit configured to input a signal current to the driven circuit (Fig. 4 and col. 13-26).

It would have been obvious at the time of invention to modify Knapp with the teachings of Suzuki, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claims 59 and 84, Knapp does not disclose the semiconductor device according to claim 18, further comprising an amplifier circuit configured to amplify a signal current outputted from the precharge circuit.

Suzuki discloses an amplifier circuit configured to amplify a signal current outputted from the precharge circuit (col. 5, line 62-col. 6, line 7).

It would have been obvious at the time of invention to modify Knapp with the teachings of Suzuki, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claims 28 and 85, Knapp does not disclose the semiconductor device according to claim 22,

wherein a gate and a drain of the second transistor are connected to each other.

Suzuki discloses wherein a gate and a drain of the second transistor are connected to each other (col. 5, lines 50-54; since connecting a transistor in such a manner causes the transistor to act as a diode, having a diode instead of a diode connected transistor would still act in the same manner).

It would have been obvious at the time of invention to modify Knapp with the teachings of Suzuki, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claims 64, 66, 79 and 86, Knapp and Suzuki do not disclose the amplifier is a source follower circuit.

However, Suzuki discloses an impedance transformation amplifier (col. 5, lines 62-64).

Since there is no benefit or advantage in the specification for choosing an amplifier circuit to be a source follower circuit, it would have been obvious to one of ordinary skill in the art at the time of invention to choose an amplifier circuit to be a source follower circuit based on a designer's choice because a source follower circuit is one type of amplifier circuit.

In regards to claims 73-74, 81 and 87, Knapp and Suzuki do not disclose the semiconductor device according to claim 1, wherein the precharge circuit is included in a current drive circuit.

However, Suzuki discloses a precharge circuit (Fig. 4 and col. 3, lines 52-65).

Since there is no benefit or advantage described in the specification for having the precharge circuit with the driven circuit, it would have been obvious at the time of

invention to choose either having the precharge circuit included with the driven circuit or separate from the driven circuit based on a design choice.

In regards to claims 88 and 89, Knapp and Suzuki disclose the semiconductor device according to claim 18, wherein a first terminal of the first switch is electrically connected to the precharge circuit, and wherein a second terminal of the first switch is electrically connected to the second switch (Knapp: Fig. 2 and Suzuki: Fig. 7; both the precharge circuit (3A) and the current source circuit (CS_{1-x}) are electrically connected to both terminals of the first switch via switch 37 and transistor 30).

4. Claims 90-93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp et al in view of Suzuki in view of Shin in further view of Tazuke (US 2002/0008687).

In regards to claims 90-93, Knapp discloses the semiconductor device according to claim 1, further comprising:

a second switch (37) configured to control an electrical connection between the signal line and the precharge circuit (col. 6, lines 35-43)

Knapp does not disclose a third switch configured to control an electrical connection between the signal line and the current source circuit; and

a fourth switch configured to control an electrical connection between the current source circuit and the precharge circuit.

Suzuki discloses a third switch (S_{1-x}) configured to control an electrical connection between the signal line and the current source circuit (Fig. 7 and col. 5, lines 9-26).

It would have been obvious at the time of invention to modify Knapp with the teachings of Suzuki, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

Knapp, Suzuki and Tazuke do not disclose a fourth switch configured to control an electrical connection between the current source circuit and the precharge circuit.

Tazuke discloses a switch (504) configured to control an electrical connection between two lines (Fig. 4 and paragraph 40). By incorporating the electrical connection of two of Tazuke into the invention of Knapp and Suzuki, one skilled in the art at the time of invention to have achieved the claimed invention, in that the precharge and current source lines would have been connected together in order to achieve line neutralization, which allows for a more effective precharge.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

Dec. 5, 2009